Today

- Data and Control Path
- Hexadecimal
- Little vs Big Endian

Assignments

- HW4 out (today)
More CPU: Datapath and Control

Three general types of operations:

- Arithmetic-logical (ALU)
- Memory reference (e.g., store and load)
- Branching

Overview of components:

For each instruction type, first two steps identical:

1. Send program counter (PC) to memory to fetch instruction
2. Read registers using fields of instruction (e.g., `addl $5 %eax`)
For an arithmetic-logical (ALU) instruction:

- result is written to a register (e.g., %eax)

For a memory-reference (load or store) instruction:

- e.g., movq $42, 8(%rax), to move 42 to mem offset + address in register
- ALU result is used as an address to load or store

For a branch instruction:

- ALU result used to calculate new PC value
Overview of components with Control Unit:

The control unit sets the control lines for the components

- inputs instruction, sets control lines
- e.g., if a memory store operation, sets MemWrite (vs MemRead or RegWrite)
- the Zero control line is used for branch-if-equal operations

Much more complexity than this ... which is covered in CPSC 431
CPU components can be decomposed into five stages:
(Remember the “Fetch-Decode-Execute” cycle ...)

1. IF: Instruction fetch
2. ID: Instruction decode and register file read
3. EX: ALU execution or address calculation
4. MEM: Data memory access
5. WB: Write back (memory or registers)

Each of the five stages can execute as a “pipeline” (like an assembly line)

- E.g., fetch new instruction while previous instruction being decoded
- Each stage occurs in one “clock cycle” of the CPU (clock cycle coordinates stages)
... from Patterson & Hennessy (Computer Org & Design)
Pipeline registers store all information resulting from each stage

- In this example, five instructions being processed at once

More advanced designs ...

- In a "superpipeline" architecture many more stages (e.g., 14-19 stages)
- In a "superscalar" architecture, multiple instructions at once per stage
- In a "multicore" architecture, multiple instructions “streams” at once